IN THE CLAIMS

1 (Original). A method of developing a response compactor comprising:

adding at least two columns to a compactor matrix for each circuit output that can produce an unknown logic value at the same time.

2 (Original). The method of claim 1 including adding at least two columns to a compactor matrix for each scan chain that can produce an unknown logic value at the same time.

3 (Original). The method of claim 2 including obtaining the maximum number of scan chains that can produce unknown logic values at the same time.

4 (Original). The method of claim 2 wherein adding at least one column to the matrix for each such scan chains that can produce an unknown logic value includes adding two columns to the matrix for each such scan chain.

5 (Original). The method of claim 2 including reducing the compactor matrix using maximum compatibility class problem.

6 (Original). The method of claim 5 including eliminating from the matrix one of at least two matching columns.

7 (Original). The method of claim 1 wherein adding at least two columns to a compactor matrix includes adding at least two columns to the compactor matrix for every combination of the number of unknown logic values plus one.

8 (Original). The method of claim 7 including adding values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has the column value zero followed by the column value one and a third row has the column values zero, zero, followed by the column value one.

9 (Original). A response compactor formed by the process including the steps of:

obtaining a number of circuit outputs that can produce unknown logic values at the same time; and

adding at least two columns to a compactor matrix for each such circuit output that can produce unknown logic values at the same time.

10 (Original). The compactor of claim 9 formed by a process wherein obtaining a number of circuit outputs that can produce unknown logic values at the same time includes determining the maximum number of circuit outputs that can produce errors at the same time.

11 (Original). The compactor of claim 9 wherein the compactor is formed by a process wherein adding at least one column to the matrix for each circuit output that can produce unknown logic values at the same time includes adding two columns to the matrix for each such circuit output.

12 (Original). The compactor of claim 9 formed by a process including reducing the compactor matrix using maximum compatibility class problem.

13 (Original). The compactor of claim 12 wherein said compactor is formed of a process including eliminating from the matrix one of at least two matching columns.

14 (Original). The compactor of claim 9 formed by a process wherein adding at least two columns to a compactor matrix includes adding at least two columns to the compactor matrix for every combination of the number of circuit outputs that can produce unknown logic values at the same time plus one.

15 (Original). The compactor of claim 14 formed by a process including adding values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has the column value zero followed by the column value one and a third row has the column value zero, zero followed by the column value one.

16 (Original). A response compactor comprising:

a plurality of exclusive OR gates arranged to handle any number of scan chains with unknown logic values.

17 (Original). The compactor of claim 14 that can handle any number of errors in the same scan cycle.

18 (Original). The compactor of claim 14 including the minimum number of scan outputs.

19 (Original). An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

add at least two columns to a compactor matrix for each scan chain that can produce an unknown logic value at the same time.

20 (Original). The article of claim 19 further storing instructions that, if executed, enable a processor-based system to obtain the maximum number of scan chains that can produce unknown logic values at the same time.

21 (Original). The article of claim 19 further storing instructions that, if executed, enable a processor-based system to add two columns to the matrix for each such unknown logic value.

22 (Original). The article of claim 19 further storing instructions that, if executed, enable the compactor matrix to be reduced using maximum compatibility class problem.

23 (Original). The article of claim 19 further storing instructions that, if executed, enable a processor-based system to eliminate from the matrix one of at least two matching columns.

24 (Original). The article of claim 19 further storing instructions that, if executed, enable a processor-based system to add at least two columns to the compactor matrix for every combination of the number of unknown logic values plus one.

25 (Original). The article of claim 23 further storing instructions that, if executed, enable a processor-based system to add values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has a column value zero followed by the column value one and the third row has the column value zero, zero, followed by the column value one.